

DSP Control Method of Single-Phase Inverters for UPS applications

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Abstract- This paper presents a new deadbeat control solution and a digital control strategy suited for high performance single-phase inverters capable to maintain very low THD of less than 1% in presence of unknown loads (linear or highly nonlinear). The method takes into account the digital model of the PWM inverter and derives a new set of gains for the voltage and current loops. The current loop gain obtained by this approach is shown to be higher than previously known and this leads to a better disturbance rejection and faster dynamic response. The control strategy was implemented on a 16-bit fixed-point DSP controller (ADMC401) and tested on a 5-KVA IGBT-based inverter switching at 20 Khz.

I. INTRODUCTION

Low distortions in the output voltage of a UPS inverter and fast dynamic response in presence of unknown distorting loads are the main attributes of any high performance inverter. The UPS applications require a pure sinusoidal waveform with a specified frequency and amplitude in presence of highly nonlinear loads such as diode or thyristor rectifiers with electrolytic capacitors. This type of load can greatly distort the output voltage waveform of an inverter based on open-loop feed-forward control with a slow rms feedback loop. Over the last 15 years many advanced control techniques have been proposed to regulate the instantaneous output voltage, thus leading to a faster response, improved total harmonic distortion (THD) content and better disturbance rejection. In general an inner fast current loop and an outer slower voltage loop are used in order to eliminate the weakly damped poles of the output LC filter [2], [8]. The method does improve the transient response and the THD content is lowered but cannot eliminate entirely the distortions produced by a nonlinear load, mainly because the analysis is based on the assumption of a linear load. Further improvements have been reported in [1] and [3] where a method to decouple the voltage and current loops and to make them independent of the load disturbance is presented. However the analysis is only accurate for an analog implementation. Repetitive control methods have received a lot of attention due to their property of removing periodic disturbances [4], [11]. Unfortunately, the repetitive controller

requires a quite complicated compensation network to ensure stability and the knowledge or the continuous automatic identification of the load is needed [11]. Additionally, the repetitive controllers are known to be slow and they are effective only if the disturbance is a harmonic of the fundamental and in some instances they can even amplify a non-harmonic disturbance [12]. Harmonic controllers have also been extensively explored [13],[14] but they apply as well only to harmonic disturbances and their transient response stretches for many fundamental cycles. Deadbeat control techniques have been applied for many years [5],[15],[16] under different versions. Although deadbeat control can theoretically provide the fastest response for a digital implementation, the method does have the disadvantage of a very high gain, which makes it extremely sensitive to the system noise. Early works [15], [16] have derived the deadbeat solutions based on linear models of the load, therefore their performances deteriorate when a nonlinear load is applied. In [5] the assumption of a linear load is dropped but the voltage and current loops are analyzed individually and the effect of discretization on the PWM inverter is not taken into account. As a result, the disturbances in the current and voltage loops cannot be totally eliminated and the THD content for nonlinear loads is still high. This paper presents a simple, reliable and easy to implement fully digital control strategy that provides excellent disturbance rejection and fast dynamics by using an accurate disturbance and feed-forward decoupling method that takes into account the effect of discretization and by employing voltage and current controllers that adapt their structure to different types of loads.

II. ANALOG AND DIGITAL DYNAMIC MODEL OF PWM INVERTER

A typical single-phase inverter is shown in figure 1, where the switches can be IGBT or MOSFET. The duty cycle of the inverter varies between $\pm 100\%$ and the amplitude of the inverter voltage, V_{input} , is proportional with the dc-link voltage V_{dc} and the duty cycle. A unipolar PWM voltage modulation type [7] is used because this method offers the advantage of effectively doubling the switching frequency of the inverter voltage, thus making the output filter smaller, cheaper and easier to implement.

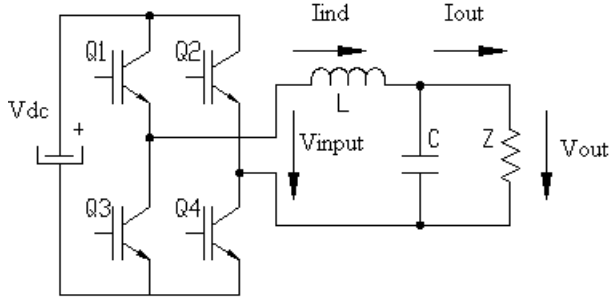


Fig.1 Single-phase PWM inverter with LC filter

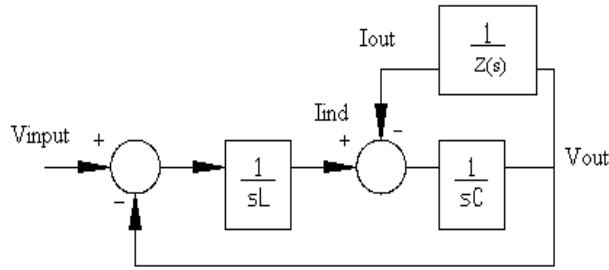


Fig.2 Analog model of the PWM inverter

According to the circuit in fig.1, the state space equations of the PWM inverter with LC filter can be written as:

$$\begin{bmatrix} \frac{dI_{ind}}{dt} \\ \frac{dV_{out}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_{ind} \\ V_{out} \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} \cdot V_{input} + \begin{bmatrix} 0 \\ -1 \end{bmatrix} \cdot I_{out} \quad (1)$$

Based on (1) and figure 1 and assuming that the switching frequency is high enough to neglect the dynamics of the inverter, the analog model of the PWM inverter with LC filter and load is shown in figure 2 where it can be seen that the output voltage acts as a disturbance on the inductor current while the output current acts as a disturbance on the output voltage. It is also assumed that the dc-link voltage variation is compensated in a feed-forward manner, therefore for frequencies well below the switching frequency (i.e. less than 1/6 of f_s) the PWM modulator stage can be eliminated from the equivalent model.

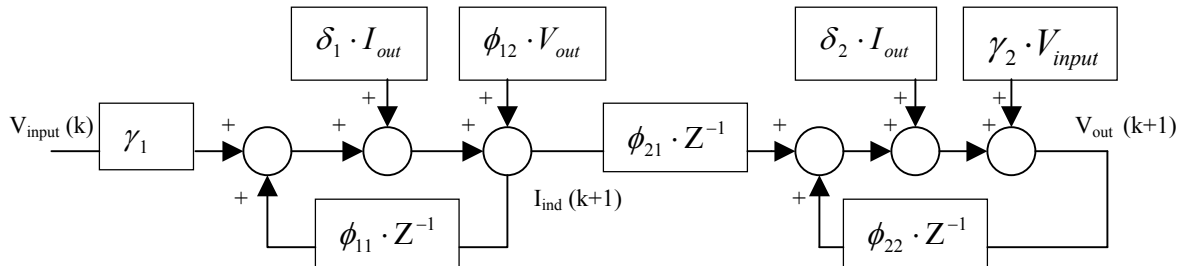


Fig.3 Digital model of the PWM inverter

For a given sampling period of T the discrete state space equations [6] of the system described by (1) can be written as:

$$x(k+1) = \Phi(T) \cdot x(k) + \Gamma(T) \cdot V_{input}(k) + \Delta(T) \cdot I_{out}(k) \quad (2)$$

$$\Phi(T) = \begin{bmatrix} \cos(\omega T) & \frac{-1}{\omega \cdot L} \cdot \sin(\omega T) \\ \frac{1}{\omega \cdot C} \cdot \sin(\omega T) & \cos(\omega T) \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \quad (3.a)$$

$$\Gamma(T) = \begin{bmatrix} \frac{1}{\omega L} \cdot \sin(\omega T) \\ 2 \sin^2(\frac{\omega T}{2}) \end{bmatrix} = \begin{bmatrix} \gamma_1 \\ \gamma_2 \end{bmatrix} \quad (3.b)$$

$$\Delta(T) = \begin{bmatrix} 2 \sin^2(\frac{\omega T}{2}) \\ \frac{-1}{\omega C} \sin(\omega T) \end{bmatrix} = \begin{bmatrix} \delta_1 \\ \delta_2 \end{bmatrix} \quad (3.c)$$

$$\omega = \frac{1}{\sqrt{LC}} \quad (4)$$

where $x(k) = \begin{bmatrix} I_{ind}(k) \\ V_{out}(k) \end{bmatrix}$ and ω is the output filter corner frequency measured in rad/sec.

From (2) and (3) the discrete data equation of the inductor current and output voltage can be written as:

$$I_{ind}(k+1) = \phi_{11} \cdot I_{ind}(k) + \phi_{12} \cdot V_{out}(k) + \gamma_1 \cdot V_{input}(k) + \delta_1 \cdot I_{out}(k) \quad (5)$$

$$V_{out}(k+1) = \phi_{21} \cdot I_{ind}(k) + \phi_{22} \cdot V_{out}(k) + \gamma_2 \cdot V_{input}(k) + \delta_2 \cdot I_{out}(k) \quad (6)$$

Based on (5) and (6) the digital model of the PWM inverter can be derived as in figure 3, where Z^{-1} represents a one sample delay.

It can be seen from this digital model that additional unwanted disturbance terms appear because of the discretization, therefore unlike in the analog model presented in figure 2, now there exist two disturbances, instead of just one, acting on the inductor current and output voltage, respectively. The equations (5) and (6) can be rewritten as:

$$V_{input}(k) = \frac{1}{\gamma_1} \cdot I_{ind}(k+1) - \frac{\phi_{11}}{\gamma_1} \cdot I_{ind}(k) - \frac{\phi_{12}}{\gamma_1} \cdot V_{out}(k) - \frac{\delta_1}{\gamma_1} \cdot I_{out}(k) \quad (7)$$

$$I_{ind}(k) = \frac{1}{\phi_{21}} \cdot V_{out}(k+1) - \frac{\phi_{22}}{\phi_{21}} \cdot V_{out}(k) - \frac{\gamma_2}{\phi_{21}} \cdot V_{input}(k) - \frac{\delta_2}{\phi_{21}} \cdot I_{out}(k) \quad (8)$$

From (7) and (8) the current disturbance and the voltage disturbance terms can be written as (9) and (10), respectively:

$$I_{dist}(k) = -\frac{\phi_{12}}{\gamma_1} \cdot V_{out}(k) - \frac{\delta_1}{\gamma_1} \cdot I_{out}(k) \quad (9)$$

$$V_{dist}(k) = -\frac{\gamma_2}{\phi_{21}} \cdot V_{input}(k) - \frac{\delta_2}{\phi_{21}} \cdot I_{out}(k) \quad (10)$$

III. PROPOSED DIGITAL CONTROL METHOD

A. New deadbeat solution

In order to achieve a fast transient response time and good disturbance rejection this paper presents a new fully digital controller, shown in figure 4, that involves an outer voltage loop and an inner inductor current loop. The disturbance terms acting on the inductor current and output voltage respectively are added at the output of the current regulator and voltage regulator respectively and assuming that the dc-link voltage variation is compensated, (7) and (8) can now be rewritten as:

$$V_{input}(k) = \frac{1}{\gamma_1} \cdot I_{ind}(k+1) - \frac{\phi_{11}}{\gamma_1} \cdot I_{ind}(k) \quad (11)$$

$$I_{ind}(k) = \frac{1}{\phi_{21}} \cdot V_{out}(k+1) - \frac{\phi_{22}}{\phi_{21}} \cdot V_{out}(k) \quad (12)$$

From figure 4, assuming that $V_{control}(k) = V_{input}(k)$ and neglecting the PI regulator and the Harmonic & Slope Calculator block whose roles will be explained later, the following equation can be obtained:

$$\left(V_{ref}(k) - V_{out}(k) \right) \cdot G_V \cdot G_I + \left(FF_1(k) - I_{ind}(k) \right) \cdot G_I + FF_2(k) = V_{input}(k) \quad (13)$$

Replacing $I_{ind}(k)$ and $I_{ind}(k+1)$ from (12) for $k = k + 1$ in equation (11) and considering that $\phi_{11} = \phi_{22}$ we derive:

$$V_{input}(k) = \frac{V_{out}(k+2) - 2 \cdot \phi_{11} \cdot V_{out}(k+1) + \phi_{11}^2 \cdot V_{out}(k)}{\phi_{21} \cdot \gamma_1} \quad (14)$$

Combining the expressions for $I_{ind}(k)$ from (12) and $V_{input}(k)$ from (14) in (13) we obtain:

$$\begin{aligned} & \left(V_{ref}(k) - V_{out}(k) \right) \cdot G_V \cdot G_I + \\ & + \left(FF_1(k) - \frac{V_{out}(k+1) - \phi_{22} \cdot V_{out}(k)}{\phi_{21}} \right) \cdot G_I + FF_2(k) = \\ & = \frac{V_{out}(k+2) - 2 \cdot \phi_{11} \cdot V_{out}(k+1) + \phi_{11}^2 \cdot V_{out}(k)}{\phi_{21} \cdot \gamma_1} \end{aligned} \quad (15)$$

Equation (15) suggests now the following values for the two feed-forward terms $FF_1(k)$ and $FF_2(k)$ respectively:

$$\begin{aligned} FF_1(k) &= \frac{V_{ref}(k+1) - \phi_{22}^{est} \cdot V_{ref}(k)}{\phi_{21}^{est}} \quad (16) \\ FF_2(k) &= \frac{V_{ref}(k+2) - 2 \cdot \phi_{11}^{est} \cdot V_{ref}(k+1) + \phi_{11}^{est2} \cdot V_{ref}(k)}{\phi_{21}^{est} \cdot \gamma_1^{est}} + \\ & + \frac{\phi_{11}^{est2} \cdot V_{ref}(k)}{\phi_{21}^{est} \cdot \gamma_1^{est}} \end{aligned} \quad (17)$$

where A^{est} is the estimated of the real value A .

Replacing (16) and (17) in (15) and after some algebraic manipulation we arrive at the following result:

$$\begin{aligned} & V_{out}(k) \cdot \left(G_V \cdot G_I - \frac{\phi_{22}}{\phi_{21}} \cdot G_I + \frac{\phi_{11}^2}{\phi_{21} \cdot \gamma_1} \right) + V_{out}(k+1) \cdot \left(\frac{G_I}{\phi_{21}} - \frac{2 \cdot \phi_{11}}{\phi_{21} \cdot \gamma_1} \right) + V_{out}(k+2) \cdot \frac{1}{\phi_{21} \cdot \gamma_1} = \\ & = V_{ref}(k) \cdot \left(G_V \cdot G_I - \frac{\phi_{22}^{est}}{\phi_{21}^{est}} \cdot G_I + \frac{\phi_{11}^{est2}}{\phi_{21}^{est} \cdot \gamma_1^{est}} \right) + V_{ref}(k+1) \cdot \left(\frac{G_I}{\phi_{21}^{est}} - \frac{2 \cdot \phi_{11}^{est}}{\phi_{21}^{est} \cdot \gamma_1^{est}} \right) + V_{ref}(k+2) \cdot \frac{1}{\phi_{21}^{est} \cdot \gamma_1^{est}} \end{aligned} \quad (18)$$

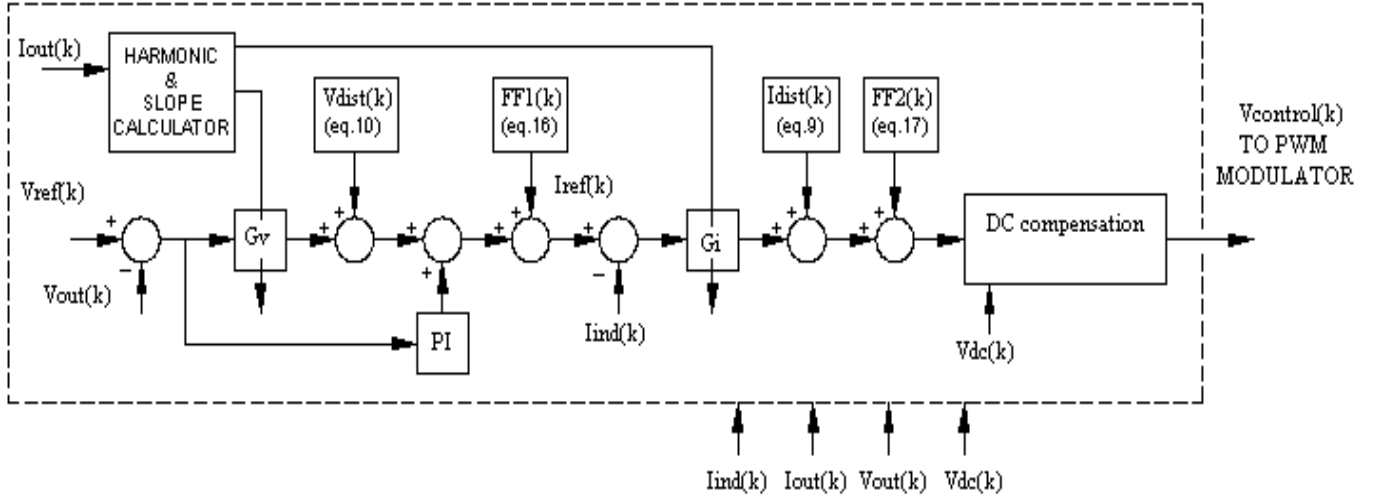


Fig.4 Proposed digital controller

It can be seen from (18) that, if all the estimated parameters are correct, a deadbeat control solution which guarantees perfect tracking of the reference voltage after two sampling periods can be achieved by setting the coefficients of $V_{ref}(k)$ and $V_{ref}(k+1)$ to zero. The two gains for the current and voltage loops obtained in this manner are:

$$G_I = \frac{2 \cdot \phi_{11}}{\gamma_1} = \frac{2 \cdot \omega \cdot L \cdot \cos(\omega \cdot T)}{\sin(\omega \cdot T)} \quad (19)$$

$$G_V = \frac{\phi_{11}}{2 \cdot \phi_{21}} = \frac{\omega \cdot C \cdot \cos(\omega \cdot T)}{2 \cdot \sin(\omega \cdot T)} \quad (20)$$

The gains defined by (19) and (20) differ fundamentally from those obtained in a previous deadbeat control implementation by others [5]. Accurate load disturbance decoupling and also sampling effect disturbance decoupling combined with the addition of new feed-forward terms have lead to a new solution for a deadbeat control. The current gain obtained by this method is higher than the one reported in [5] while the voltage gain is smaller than the one reported in the same work. For high switching/sampling frequency it can be seen that G_I , G_V approach $\frac{2 \cdot L}{T}$ and $\frac{C}{2 \cdot T}$ respectively as compared with $\frac{L}{T}$ and $\frac{C}{T}$ respectively found in [5] when the resistances of inductor and output capacitors are neglected. The dynamic performances are primarily given by the inner current loop and the higher gain given by (19) leads to a faster response time and lower THD in presence of highly nonlinear loads. The term $FF_1(k)$ corresponds to the output capacitor current reference for digital control and it can be easily shown that only when $\omega \cdot T$ approaches zero, $FF_1(k)$ is equal to the output capacitor current obtained by forward Euler transform. It is interesting to note that (18) corresponds to the analog

controller proposed in [3] which was shown to exhibit perfect tracking for the ideal case. However, for this digital approach perfect tracking of the reference can only be obtained after two sampling periods, which is consistent with the deadbeat control theory for a second order system.

B. Harmonic and slope calculator

Although the proposed control method can ideally track the reference after two sampling periods, there are some factors that affect the performances such as: imperfect estimation or variation of inverter parameters (especially inductor value can vary under heavy nonlinear loads or during a momentary overload), offset and delay of the sensors, errors in A/D converter, switching time and conduction voltage drop of the IGBT's, quantization noise (especially when a 16-bit fixed point DSP is used), delay due to the computation time, etc. Also, the high gain of the controllers makes this approach extremely sensitive to the noise unless special precautions are taken. We must emphasize here that the use of such high gains obtained by (19) and (20) is only justified if there is a nonlinear load. If the load is reactive a traditional approach with a voltage loop (PI type controller) and an inner current loop (P or PI type controller) [1],[2],[3],[8] gives excellent results. The addition of the digital disturbance decoupling as described here improves the response and increases the robustness. The primary goal was to implement the solution on a low cost 16-bit fixed point DSP controller therefore we adopted a simple strategy that adapts the voltage and current controllers to the type of the load. The strategy is illustrated by the flowchart shown in figure 7. It can be seen that if the output current is determined to have only a reactive component then a PI voltage controller and a P current controller are employed (details for this type can be found in [1], [2],[3],[8]). It has been shown in [8] that the bandwidth of a current controller with a gain of K is approximately

$f_c = \frac{K}{2 \cdot \pi \cdot L}$ and given the high switching/sampling frequency of the inverter, a bandwidth of 4 KHz is selected. This high bandwidth is sufficient for eliminating the disturbances produced by a reactive load. Next we will briefly review a very simple method for calculating the reactive and harmonic components of the current [9]. The output current is made up of the following terms (no dc component is assumed):

$$I_{out} = I_{sin} + I_{cos} + I_{harmonics} \quad (21)$$

$$I_{sin} = I_S \cdot \sin(\omega \cdot t) \quad (22)$$

$$I_{cos} = I_C \cdot \cos(\omega \cdot t) \quad (23)$$

To find the in-phase component we have to multiply (21) by a sinusoid in phase with the output voltage and the following equation can be written:

$$I_{out} \cdot \sin(\omega \cdot t) = I_S \cdot \left(\frac{1 - \cos(2 \cdot \omega \cdot t)}{2} \right) + \dots + \text{(Higher frequency order ac terms).} \quad (24)$$

By passing (24) through a low pass filter we can extract the value of I_S and by multiplication with the sinusoid in phase with the output voltage we can obtain the in phase component. However, this approach has the inherent disadvantages of an open loop method and therefore a more robust solution is shown in figure 5. This is a closed loop solution, which is capable of removing the magnitude error due to the low pass filter. A detailed analysis of this method can be found in [9]. Obviously a similar approach is used to extract the quadrature component of the current and the closed loop scheme is depicted in figure 6. It should be noted that the calculation of the reactive and harmonic components of the current is required anyway if parallel operation without any control interconnections is desired [10], so this does not imply any overhead in a high performance inverter. If the load is determined to have a nonlinear component a simple slope calculator determines a variable proportional with dI_{out}/dt by calculating the difference between two consecutive output current samples $I_{out}(k) - I_{out}(k-1)$. If this variable is found to be greater than a preset threshold then the gain controllers defined by (19) and (20) are selected in order to quickly respond to a highly nonlinear load. Although extremely simple in its nature this mechanism is essential for a reliable operation since a nonlinear load may draw current spikes for a limited time only during a fundamental period (such is the case of diode rectifiers with electrolytic capacitors) and high frequency oscillations due to the high gain of the controllers in presence of inherent errors may occur during the time the current is zero or it has only a small variation. Figure 8 depicts the proposed control method when the slope calculator is disabled and as expected, a high frequency noise is superimposed on the output voltage and

the THD is 5.4%. When the slope calculator is enabled the high frequency noise is removed as shown in figure 9 and the THD% has dropped to 0.8 % in presence of a nonlinear load (load power factor = 0.49, P = 1.2 kW, S = 2.4kVA, R = 2.1kVAR, output current THD = 86.4%, output peak current = 96.5A, output rms current = 20A). If a DC-link feed-forward compensation is not used, therefore reducing the number of sensors required, a simple PI regulator from the output voltage as shown in figure 4 will maintain excellent steady-state regulation.

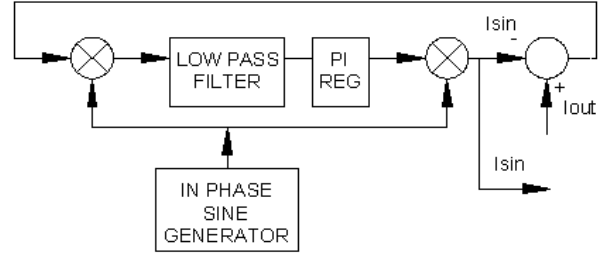


Fig.5 Closed loop scheme for calculating the in-phase current

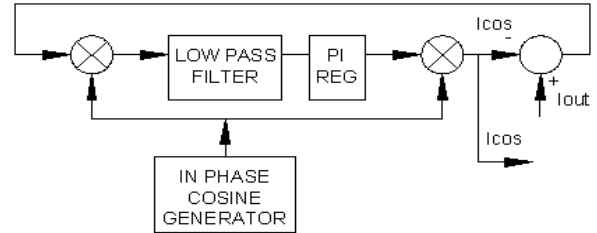


Fig.6 Closed loop scheme for calculating the quadrature current

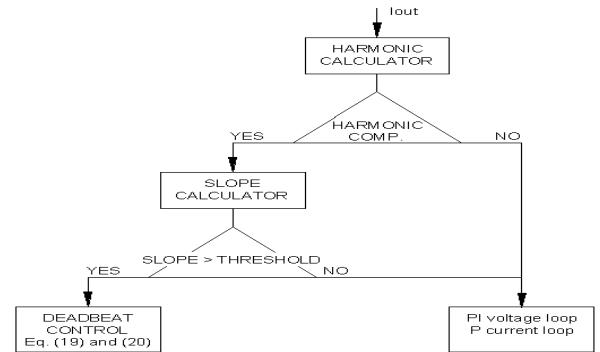


Fig.7 Flowchart for the adopted control strategy

IV. EXPERIMENTAL RESULTS

The proposed digital method has been implemented using a 16-bit fixed point DSP-based controller ADMC401(Analog Devices). This 26 MIPS single-chip DSP controller is extremely suitable for easy and inexpensive implementation of various high performance digital control algorithms because it includes all the facilities required in a voltage and

current control loop such as: 12-bit flash A/D with 1.8 μ sec conversion time for all 8 channels, high resolution PWM unit, 1-kbyte RAM for data memory, 2-kbyte RAM for program memory, 2-kbyte ROM program memory for boot routines and debug features, 2 event capture channels, encoder interface, etc. A single-phase 60 hz, 120V IGBT-based inverter rated for 5-KVA with a nominal DC-link voltage of 300V switching at 20 khz was used to verify the proposed control method. The parameters of the filter are: $L = 200\mu\text{H}$, $C = 100\mu\text{F}$ and the nonlinear load consisted of a full-wave diode bridge rectifier with an electrolytic capacitor of 3300 μF and load resistance of 20 ohm. In all cases the THD was measured using a FLUKE 43B Harmonic Analyzer. Sampling frequency was chosen 40 khz and the PWM pulses are updated twice per carrier (double edged unsymmetrical PWM) in order to minimize the computational delay. Figure 11 depicts a transient step with a nonlinear load showing excellent dynamic response. Figures 12 and 13 depict operation with linear load (transient from 0 to 40 A rms and steady state current of 40A rms respectively) and the THD is found to be 1%). A very interesting situation is shown in figure 14 (and detailed in figure 15) where it is recorded the transient turn-on of a single-phase 2.5HP peak compressor. Although the steady-state current is only 10A rms, the turn-on inrush current reaches 125A and despite such a heavy nonlinear load the inverter performs very well maintaining a very low THD of 1.1 % even during the transient turn-on when the current has a very unpredictable waveform. Also it is important to note that the DC-link feed-forward compensation was not implemented in the experimental setup, yet excellent result have been obtained and the regulation was better than 0.3%.

V. CONCLUSIONS

This paper presented a simple, yet extremely effective digital control method for a single-phase inverter. Accurate decoupling that takes into account the effect of discretization and the addition of a new feed-forward term lead to a new deadbeat control solution capable to effectively reject the disturbances of a heavy nonlinear load. A simple harmonic and slope calculator determines the type of load and schedules the gains of the voltage and current loops improving the quality of the sine wave. The solution has been tested on a single-chip DSP-based controller that implements all the algorithms described, including A/D conversion and PWM pulse generation, in less than 25 μ sec although no attempt was made to optimize the code. The software program was written in ANALOG DEVICE's assembly language for 16-bit fixed-point digital signal processors (ADSP2100 family). The experimental work on a 5-KVA inverter confirmed the validity and feasibility of this new approach.

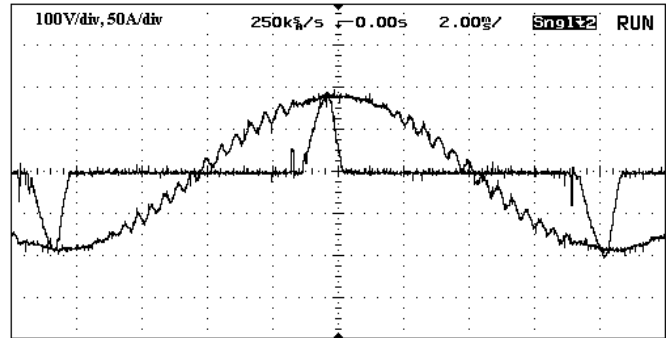


Fig.8 Output voltage (100V/div) and output current (50A/div) without the slope calculator, THD = 5.4%.

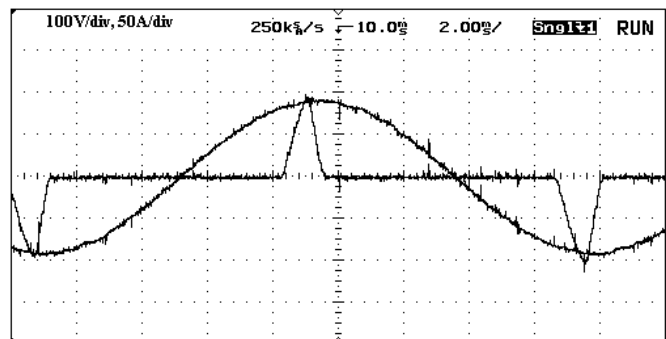


Fig.9 Output voltage (100V/div) and output current (50A/div) with the slope calculator enabled, THD = 0.8%.

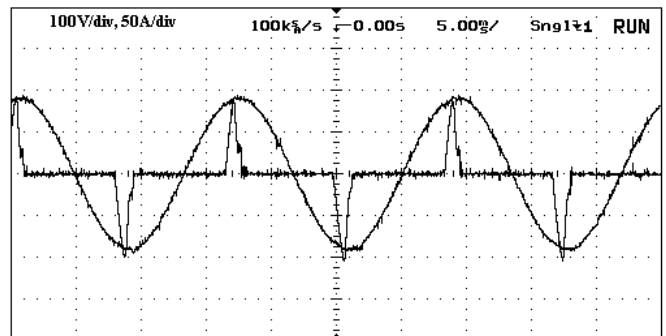


Fig.10 Output voltage (100V/div) and output current (50A/div) during steady-state operation with a nonlinear load, THD = 0.8%.

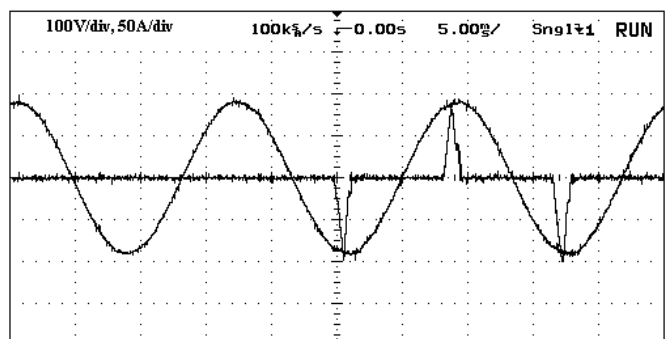


Fig.11 Output voltage (100V/div) and output current (50A/div) during transient with a nonlinear load, THD = 0.8%..

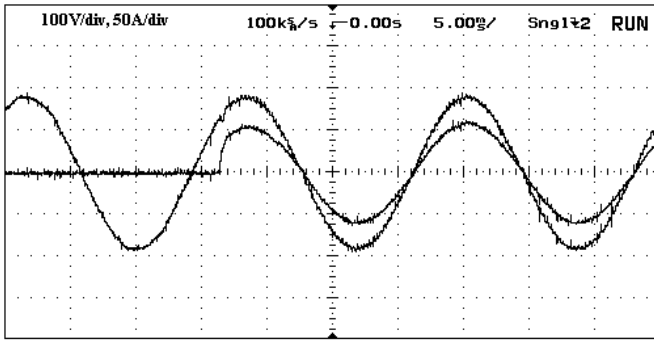


Fig.12 Output voltage (100V/div) and output current (50A/div) during transient with a linear load, THD = 1%.

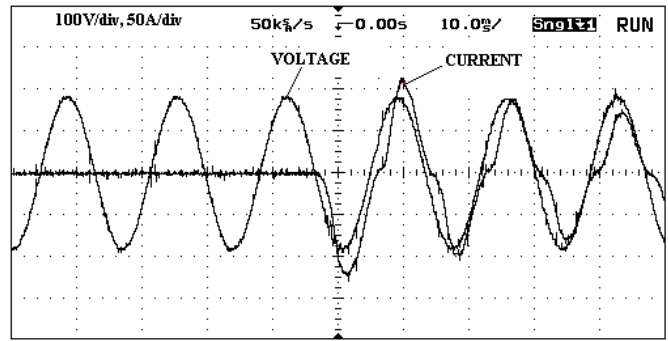


Fig.14 Output voltage (100V/div) and output current (50A/div) during transient with a compressor load, THD = 1.1%.

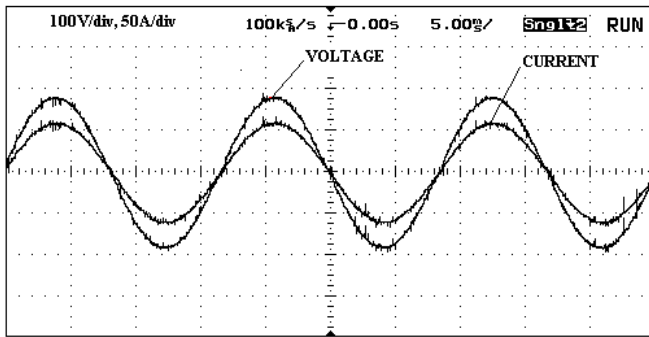


Fig.13 Output voltage (100V/div) and output current (50A/div) during transient with a linear load, THD = 1%.

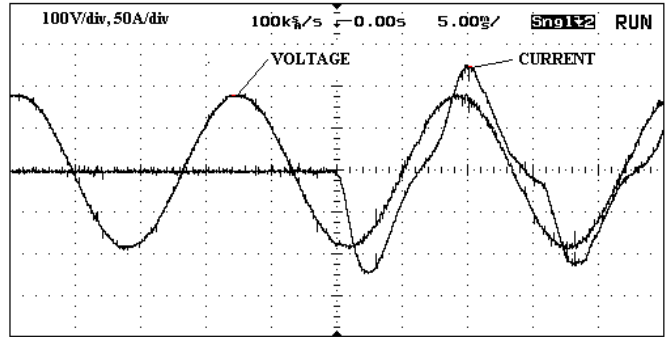


Fig.15 Output voltage (100V/div) and output current (50A/div) during transient with a compressor load, THD = 1.1%.

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