

DSP Control of 400 Hz Inverters for Aircraft Applications

Liviu Mihalache, Member IEEE
Power Conversion Technologies Inc.
Harmony, USA
e-mail: lm@gopcti.com

Abstract—This paper presents a fully digital control method that can be used for inverters used in 400 Hz aircraft ground power units. The method presents an ideal tracking controller that incorporates the computational delay as well as the quantization effects. It uses an observer for the output current third, fifth and seventh harmonics in order to achieve decoupling between the voltage and current loops thus leading to a low THD content in presence of non-linear loads. The implementation of the observer is reduced to IIR filters with normal architecture that have minimum round off errors. The control method is implemented on a 16-bit single chip DSP-based controller from Analog Devices (ADMC401) and tested on a single-phase 10kva IGBT-based inverter prototype showing almost complete elimination of the third, fifth and seventh harmonics from the output voltage.

I. INTRODUCTION

It is well known that non-linear loads can distort the output voltage of a voltage inverter even if instantaneous control is used. Thus, many advanced control strategies have been proposed over the last decade in order to maintain a low THD content in presence of nonlinear loads such as: sliding mode control, repetitive control, dead-beat control, selective harmonic control, dissipativity-based control, optimum state space control etc. However, the vast majority of them have dealt with 50/60 Hz inverters for UPS applications and few of them have focused on the 400 Hz inverters used in Ground Power Units (GPU) for aircraft applications [8], [12]. The main difference between the GPU and the UPS type inverters is that the frequency band between the fundamental and the harmonics generated by the inverter itself and by the nonlinear load is very low; therefore, it becomes very difficult to maintain a low THD content for a GPU inverter. The computational delay also cannot be ignored due to the high fundamental frequency where the effects are much more significant than in the case of 50/60 Hz inverters. Early ground power units (GPU) were designed using optimized modulation schemes that eliminated or reduced the amount of harmonic distortion, thus reducing the size of the output filter. In the very high power ranges the traditional method of choice was to use step wave inverters where multiple inverters working at low switching frequency are added together via special transformers to develop an output voltage of 12, 24 or even 48 pulses. The step wave inverters require a large number of semiconductors thus decreasing the reliability and increasing the cost. Regardless of the choice, these types of

inverters are difficult to control resulting in a very slow response to load steps. In the past, the control requirements were quite low and a true rms voltage control calculated once per fundamental was enough to achieve satisfactory performance. However, today's demands are much higher and generally require a higher control bandwidth and operation in the presence of highly nonlinear loads and unsymmetrical and/or single-phase loads connected line to line and line to ground. Rapid advances in the aircraft industry has led to an increase of electronic equipment on board airplanes; therefore, the amount of nonlinear load continues to grow, and the ability to maintain clean power in presence of distorting load becomes more and more challenging as the power level increases. Today's advance of power semiconductors and digital signal processors (DSP) with enhanced computational power make possible the development of highly advanced algorithms in order to provide clean power in the presence of highly distorting and unsymmetrical loads. The semiconductor's technology makes possible the use of PWM IGBT-based inverters switching at 16 to 20 KHz. Here, the output filter becomes very small and a higher control bandwidth is possible because the corner frequency of the output filter is now pushed farther from the 400 Hz fundamental. The use of single chip digital signal processors controllers capable of 20 to 150 MIPS (million instructions per second) with on-chip analog /digital converter, memory, PWM channels, event capture units and communication channels lead to a very compact, reliable, and fully digital implementation of a modern GPU. This paper focuses on the DSP control of a 400 Hz single-phase inverter, which can be used as a stand-alone unit, or in a medium to high power three-phase inverter made-up of three single-phase inverters with the advantage of lower semiconductor stress and lower harmonics content. The method may also be extended to standard three-phase inverters with six switches with the advantage of excellent behavior in the presence of an unbalanced load. The proposed method takes into account computational effects and develops a disturbance decoupling method that leads to the rejection of the third, fifth and seventh harmonics from the output voltage resulting in much lower THD content in the presence of non-linear or unbalanced loads.

II. MODELS OF THE ANALOG AND DIGITAL PWM INVERTER

A typical single-phase inverter with IGBT switches is shown in Fig 1. The duty cycle of the inverter varies between

$\pm 100\%$ and the amplitude of the inverter voltage, V_{input} , is proportional with the dc-link voltage V_{dc} and the duty cycle. A unipolar PWM voltage modulation type [6] is used because this method offers the advantage of effectively doubling the switching frequency of the inverter voltage, thus making the output filter smaller, cheaper and easier to implement. The DC-link voltage is usually provided by either a single/three-phase diode rectifier or by a PWM rectifier in order to improve the power factor and to reduce the line current harmonics.

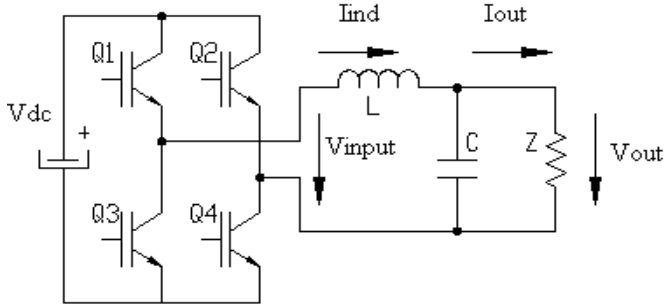


Fig. 1. Single-phase PWM inverter with LC filter.

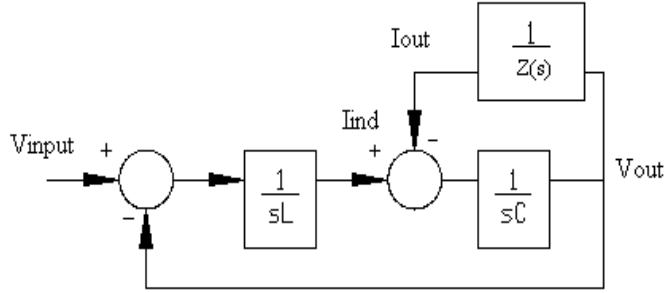


Fig. 2. Analog model of the PWM inverter.

According to the circuit in Fig. 1, the continuous time state space equations of the PWM inverter with LC filter can be written as:

$$\begin{bmatrix} \frac{dI_{ind}}{dt} \\ \frac{dV_{out}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} I_{ind} \\ V_{out} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{input} + \begin{bmatrix} 0 \\ -\frac{1}{C} \end{bmatrix} I_{out} \quad (1)$$

Based on (1) and Fig. 1 the analog model of the PWM inverter with LC filter and load is shown in Fig. 2 where it can be seen that the output voltage acts as a disturbance on the inductor current while the output current acts as a disturbance on the output voltage. For a given sampling period of T the discrete state space equations [5] of the system described by (1) can be written as:

$$x(k+1) = \Phi(T)x(k) + \Gamma(T)V_{input}(k) + \Delta(T)I_{out}(k) \quad (2)$$

$$\Phi(T) = \begin{bmatrix} \cos(\omega T) & \frac{-1}{\omega \cdot L} \cdot \sin(\omega T) \\ \frac{1}{\omega \cdot C} \cdot \sin(\omega T) & \cos(\omega T) \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \quad (3)$$

$$\Gamma(T) = \begin{bmatrix} \frac{1}{\omega L} \cdot \sin(\omega T) \\ 2 \sin^2\left(\frac{\omega T}{2}\right) \end{bmatrix} = \begin{bmatrix} \gamma_1 \\ \gamma_2 \end{bmatrix} \quad (4)$$

$$\omega = \frac{1}{\sqrt{LC}} \quad (5)$$

$$\Delta(T) = \begin{bmatrix} 2 \sin^2\left(\frac{\omega T}{2}\right) \\ \frac{-1}{\omega C} \sin(\omega T) \end{bmatrix} = \begin{bmatrix} \delta_1 \\ \delta_2 \end{bmatrix} \quad (6)$$

where $x(k) = \begin{bmatrix} I_{ind}(k) \\ V_{out}(k) \end{bmatrix}$ and ω is the output filter corner frequency measured in rad/sec.

From (2) to (6) the discrete data equation of the inductor current and output voltage can be written in the form of the following two equations:

$$I_{ind}(k+1) = \phi_{11}I_{ind}(k) + \phi_{12}V_{out}(k) + \gamma_1V_{input}(k) + \delta_1I_{out}(k) \quad (7)$$

$$V_{out}(k+1) = \phi_{21}I_{ind}(k) + \phi_{22}V_{out}(k) + \gamma_2V_{input}(k) + \delta_2I_{out}(k) \quad (8)$$

It can be seen from this digital model that additional unwanted disturbance terms appear because of the discretization, therefore unlike in the analog model presented in Fig. 2, now there exist two disturbances, instead of just one, acting on the inductor current and output voltage, respectively. The equations (7) and (8) can be rewritten as:

$$V_{input}(k) = \frac{1}{\gamma_1}I_{ind}(k+1) - \frac{\phi_{11}}{\gamma_1}I_{ind}(k) - \frac{\phi_{12}}{\gamma_1}V_{out}(k) - \frac{\delta_1}{\gamma_1}I_{out}(k) \quad (9)$$

$$I_{ind}(k) = \frac{1}{\phi_{21}}V_{out}(k+1) - \frac{\phi_{22}}{\phi_{21}}V_{out}(k) - \frac{\gamma_2}{\phi_{21}}V_{input}(k) - \frac{\delta_2}{\phi_{21}}I_{out}(k) \quad (10)$$

From (9) and (10) the current and the voltage disturbance terms can be written as (11) and (12), respectively:

$$I_{dist}(k) = -\frac{\phi_{12}}{\gamma_1}V_{out}(k) - \frac{\delta_1}{\gamma_1}I_{out}(k) \quad (11)$$

$$V_{dist}(k) = -\frac{\gamma_2}{\phi_{21}}V_{input}(k) - \frac{\delta_2}{\phi_{21}}I_{out}(k) \quad (12)$$

III. PROPOSED DIGITAL CONTROL APPROACH

In order to achieve a fast transient response time and good disturbance rejection, this paper presents a new fully digital

controller, shown in Fig. 3, that involves an outer voltage loop and an inner inductor current loop.

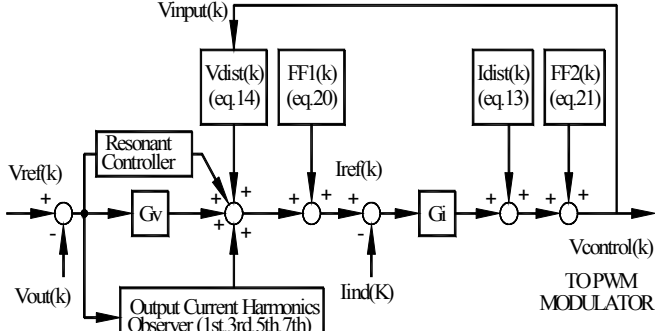


Fig. 3. Proposed digital controller.

The disturbance terms acting on the inductor current and output voltage respectively are measured or estimated and added at the output of the current regulator and voltage regulator respectively. However since the output current is not measured the two disturbance terms given by (11) and (12) are re-written as:

$$I_{dist}(k) = -\frac{\phi_{12}}{\gamma_1} V_{out}(k) \quad (13)$$

$$V_{dist}(k) = -\frac{\gamma_2}{\phi_{21}} V_{input}(k) \quad (14)$$

It is seen that the output current was dropped from the two terms and an estimation of the main output current harmonics (third, fifth and seventh) will be added to (12) since $\delta_2 = \Phi_{21}$ while the component proportional with the output current is usually much smaller and it can be ignored in (11). The control voltage used by the PWM modulator approximates the input voltage of the inverter V_{input} in Fig. 1 where it is assumed that dead-time effects are also compensated in a dynamic manner as described in [11]. The estimation for the main output current harmonics and the integrating resonant controller are discussed in depth in section IV and we will assume for now a perfect disturbance decoupling. With this assumption and considering that the dc-link voltage variation is feed-forward compensated, (9) and (10) can now be rewritten as:

$$V_{input}(k) = \frac{1}{\gamma_1} I_{ind}(k+1) - \frac{\phi_{11}}{\gamma_1} I_{ind}(k) \quad (15)$$

$$I_{ind}(k) = \frac{1}{\phi_{21}} V_{out}(k+1) - \frac{\phi_{22}}{\phi_{21}} V_{out}(k) \quad (16)$$

From Fig. 3, assuming that $V_{control}(k-1) = V_{input}(k)$ to take into account a one sample delay for computations the following equation can be obtained:

$$(V_{ref}(k) - V_{out}(k))G_V G_I + (FF_1(k) - I_{ind}(k))G_I + FF_2(k) = V_{control}(k) \quad (17)$$

Replacing $I_{ind}(k)$ and $I_{ind}(k+1)$, from (16) for $k = k + 1$ in equation (15) and considering that $\phi_{11} = \phi_{22}$ we derive the following expression for the V_{input} :

$$V_{input}(k) = \frac{V_{out}(k+2) - 2\phi_{11}V_{out}(k+1) + \phi_{11}^2V_{out}(k)}{\phi_{21}\gamma_1} \quad (18)$$

Combining the expressions for $I_{ind}(k)$ from (16) and $V_{input}(k)$ from (18) in (17) we obtain:

$$\begin{aligned} & (V_{ref}(k) - V_{out}(k))G_V G_I + \\ & + \left(FF_1(k) - \frac{V_{out}(k+1) - \phi_{22}V_{out}(k)}{\phi_{21}} \right) G_I + FF_2(k) = \\ & = \frac{V_{out}(k+3) - 2\phi_{11}V_{out}(k+2) + \phi_{11}^2V_{out}(k+1)}{\phi_{21}\gamma_1} \quad (19) \end{aligned}$$

Equation (19) suggests now the following values for the two feed-forward terms $FF_1(k)$ and $FF_2(k)$ respectively:

$$FF_1(k) = \frac{V_{ref}(k+1) - \phi_{22}^{est}V_{ref}(k)}{\phi_{21}^{est}} \quad (20)$$

$$\begin{aligned} FF_2(k) = & \frac{V_{ref}(k+3) - 2\phi_{11}^{est}V_{ref}(k+2)}{\phi_{21}^{est}\gamma_1^{est}} + \\ & + \frac{\phi_{11}^{est2}V_{ref}(k+1)}{\phi_{21}^{est}\gamma_1^{est}} \quad (21) \end{aligned}$$

Throughout this paper we will consider that A^{est} represents the estimation of the real value A . Note that the $FF_1(k)$ term differs significantly from the traditional capacitor current term because ωT cannot be approximated to zero for high fundamental frequency. Replacing (20) and (21) in (19), with some algebraic manipulation we arrive at the following result:

$$\begin{aligned} & V_{ref}(k)(G_V G_I \phi_{21}^{est} \gamma_1^{est} - \phi_{22}^{est} \gamma_1^{est} G_I) + V_{ref}(k+1) \cdot \\ & \cdot (\phi_{11}^{est2} + \gamma_1^{est} G_I) - 2V_{ref}(k+2)\phi_{11}^{est} + V_{ref}(k+3) = \\ & = V_{out}(k)(G_V G_I \phi_{21} \gamma_1 - \phi_{22} \gamma_1 G_I) + V_{out}(k+1) \cdot \\ & \cdot (\phi_{11}^2 + \gamma_1 G_I) - 2V_{out}(k+2)\phi_{11} + V_{out}(k+3) \quad (22) \end{aligned}$$

We can now apply the Z-transform to (22) and we obtain:

$$\begin{aligned} & V_{ref}(z)[G_V G_I \phi_{21}^{est} \gamma_1^{est} - \phi_{22}^{est} \gamma_1^{est} G_I + z(\gamma_1^{est} G_I + \\ & + \phi_{11}^{est2}) - 2z^2 \phi_{11}^{est} + z^3] = V_{out}(z)[G_V G_I \phi_{21} \gamma_1 - \\ & - \phi_{22} \gamma_1 G_I + z(\gamma_1 G_I + \phi_{11}^2) - 2z^2 \phi_{11} + z^3] \quad (23) \end{aligned}$$

From (23), one can easily see that the transfer function can be written in following form, where $H^{est}(z)$ is the estimated value of the real function $H(z)$:

$$\frac{V_{out}(z)}{V_{ref}(z)} = \frac{H^{est}(z)}{H(z)} \quad (24)$$

To guarantee the stability of the system one can apply the Jury's stability criterion [5] for the characteristic equation of the digital system described by the transfer function given by (23) and (24):

$$z^3 - 2\phi_{11}z^2 + (G_I\gamma_1 + \phi_{11}^2)z + G_V G_I \phi_{21}\gamma_1 - \phi_{22}G_I\gamma_1 = 0 \quad (25)$$

After some lengthy algebraic manipulations we can reach the following conditions that guarantee the stability of the system:

$$1 - a_3^2 > 0 \quad (26)$$

$$(1 - a_3^2 - a_2 + a_1 a_3)(1 - a_3^2 + a_2 - a_1 a_3) > 0 \quad (27)$$

$$(1 - a_3 + a_2 - a_1)(1 + a_3 + a_2 + a_1) > 0 \quad (28)$$

We have used the following notations:

$$a_1 = -2\phi_{11} \quad (29)$$

$$a_2 = G_I\gamma_1 + \phi_{11}^2 \quad (30)$$

$$a_3 = G_V G_I \phi_{21}\gamma_1 - \phi_{22}G_I\gamma_1 \quad (31)$$

Given the stability requirements found, one can determine first the current gain and then the voltage gain is determined so as to satisfy the conditions required by (26) - (28) in order to guarantee the overall stability of the system. For a given current gain solving conditions (26) - (28) is rather complicated, therefore a more natural approach is to determine the root-locus of (25) using traditional methods [4] or a computer software package in order to establish the voltage gain stability limits. A model for the current loop is depicted in Fig. 4 where the one sample delay due to the DSP calculations has been taken into account. The digital model also shows the feed-forward term FF2 although it does not have any effect in the stability of the current loop.

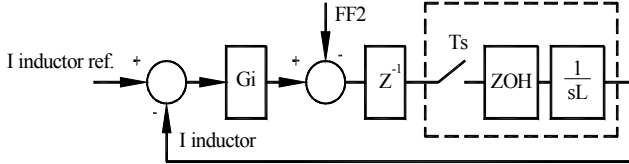


Fig. 4. Digital model of the inner current loop.

A zero order holder is used to determine the digital equivalent model of the current loop; it is easy to show that the transfer function of the current loop can be written as:

$$\frac{I_{inductor}}{I_{ref}} = \frac{T(G_I + FF_2)}{Lz(z-1) + TG_I} \quad (32)$$

The two roots of the characteristic equation given by the transfer function (32) can be written as:

$$z_{1,2} = \frac{1 \pm \sqrt{1 - \frac{4TG_I}{L}}}{2} \quad (33)$$

To guarantee the stability of the current loop, the two poles have to lie inside the unity circle, which can be shown to lead to the following simple condition for the current loop gain:

$$G_I < G_{lim} = \frac{L}{T} \quad (34)$$

One must emphasize that the effect of the one sample delay in the current loop is very important in establishing the

maximum allowable current gain. Traditionally, the current gain as given by G_{lim} is used for a dead-beat control implementation [3] if no computational delay is assumed. The result from (34) shows that a one-sample delay will transform a first order system with a pole in the origin, that is a dead-beat control, into a second order system with two complex conjugate poles located on the unity circle and the stability cannot be guaranteed. Therefore, the current gain needs to be lowered in order to satisfy the condition (34). A gain closer to G_{lim} will give a higher current bandwidth but will also be less robust since the two poles will be located close to the stability limit. On the other hand, a smaller current gain will make the system more robust but the current bandwidth will be reduced and as a result, the output impedance of the inverter will be increased; thus, the distortion will increase in the presence of nonlinear loads. Clearly, a trade-off between the two is needed and we have experimentally seen that a gain of αG_{lim} where α has values between 0.8 and 0.9 gives good results.

IV. OUTPUT CURRENT OBSERVER AND RESONANT CONTROLLER

We will begin the derivation of the output current observer for the third, fifth and seventh harmonic by re-writing (2) in the form:

$$x(k+1) = \Phi(T)x(k) + \Gamma(T)V_{input}(k) + \Delta(T)w_{1j}(k) \quad (35)$$

In the above expression we will assume that $w_{1j}(k)$ is an unknown disturbance, that is, one of the harmonic components of the output current that needs to be estimated. Although the output current can contain a large and unknown number of harmonics, we will only estimate up to seventh harmonic component due to practical limitations in the switching/sampling frequency. Therefore the output current can be written in the form:

$$I_{out}(t) = \sum I_j \sin(\omega_j \cdot t + \varphi_j) \quad j=1,3,5,7 \quad (36)$$

An estimator for the output disturbance can be expressed as a recursive first order equation that depends on the difference between the reference and the feedback signal [5]:

$$w_{1j}(k+1) = \Phi_{1j}w_{1j}(k) + c_{1j}e(k) \quad (37)$$

$$e(k) = V_{ref}(k) - V_{out}(k) \quad (38)$$

Since the term $w_{1j}(k)$ represents any one of the output current harmonics component from (36) one can write a simple expression for $w(k)$ as:

$$w_{1j}(k) = I_j \sin(\omega_j \cdot kT + \varphi_j) \quad (39)$$

Let's now consider a fictive disturbance component written as a quadrature component of the real component $w_{1j}(k)$:

$$w_{2j}(k) = -I_j \cos(\omega_j \cdot kT + \varphi_j) \quad (40)$$

Similar to (37) one can write an estimator for w_{2j} as:

$$w_{2j}(k+1) = \Phi_{2j}w_{2j}(k) + c_{2j}e(k) \quad (41)$$

One can now form a vector $v(k)$ with two components, $w_{1j}(k)$ and $w_{2j}(k)$, satisfying the following second order recursive equation:

$$v_j(k+1) = \Phi_{Vj}v_j(k) + C_j e(k) \quad (42)$$

$$v_j(k) = \begin{bmatrix} w_{1j}(k) \\ w_{2j}(k) \end{bmatrix} \quad (43)$$

$$\Phi_{Vj} = \begin{bmatrix} \cos(\omega_j T) & -\sin(\omega_j T) \\ \sin(\omega_j T) & \cos(\omega_j T) \end{bmatrix} \quad (44)$$

$$C_j = \begin{bmatrix} c_{1j} \\ c_{2j} \end{bmatrix} = c_j \begin{bmatrix} \sin(\omega_j T) \\ 2 \sin^2\left(\frac{\omega_j T}{2}\right) \end{bmatrix} \quad (45)$$

Comparing (3) - (6) with (42) - (45), one can see that the observer for the output current harmonic can be represented as a simple resonant LC circuit as in Fig. 5, satisfying (46) where the two components of the vector $v(k)$ are the resonant current and resonant voltage respectively and the input to the circuit is proportional to the error between the reference and the output voltage. Obviously one such estimator has to be implemented for each of the output current harmonic components considered, that is fundamental to the seventh harmonic.

$$L = C = \frac{1}{\omega_j} \quad (46)$$

With the notations from Fig. 5, it is obvious that the following correspondence holds:

$$I_{res}(k) = w_{1j}(k) \quad (47)$$

$$V_{res}(k) = w_{2j}(k) \quad (48)$$

$$V_{in}(k) = c_j e(k) \quad (49)$$

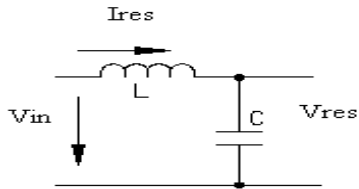


Fig. 5. Equivalent resonant LC circuit for the output current harmonic observer.

One can see now that the problem is reduced to that of finding the resonant current of the LC circuit when the input is given by (49). Writing the transfer function from the $E(s)$ to $I_{res}(s)$, one obtains:

$$H_{LC}(s) = \frac{I_{res}(s)}{E(s)} = c_j \frac{s\omega_j}{s^2 + \omega_j^2} \quad (50)$$

It is easy to recognize that (50) is the expression of a selective filter which is also used as an integrating resonant controller [1], [2]. Unlike regular integrating controllers these controllers have the advantage of an infinite gain at the frequency of interest and they are known to achieve zero phase and amplitude error when used to regulate AC signals. Therefore, the observer has the same structure as an integrating resonant controller, which is implemented as a second order IIR filter through (42) - (45). One can easily see that the IIR filter with the matrix given by (44) satisfies the commutative property, therefore it is called a normal IIR filter, and it can be shown to have minimum coefficient round-off and minimal noise gain [9], [10]. This is important in the case of a low-cost fixed-point DSP implementation where an implementation of (50) as

a standard biquad IIR filter will be sensitive to coefficients errors. The main problem becomes now selecting a proper integrating constant, c_j , for every harmonic frequency and for the fundamental. From (47) and (50) one can write:

$$W_{1j}(s) = c_j \frac{s\omega_j}{s^2 + \omega_j^2} \cdot E(s) \quad (51)$$

Assuming that the every harmonic voltage component is low, the filters given by (50) have a gain of almost zero outside the frequency ω_j , therefore, it is possible to replace $E(s)$ with $E_j(s)$, the output voltage harmonic, where:

$$E_j(k) = V_j \sin(\omega_j \cdot kT + \varphi_{vj}) \quad (52)$$

Replacing the continuous time equivalent of (39) and (52) in (51) and assuming for simplicity that $\varphi_j = \varphi_{vj} = 0$, one can obtain the following result in the time domain:

$$I_j \sin(\omega_j t) = c_j V_j \frac{t\omega_j}{2} \sin(\omega_j t) \quad (53)$$

We can specify now a desired response time for each harmonic observer and the integrating constant becomes:

$$c_j = \frac{2I_{j\max}}{V_{j\max} \cdot t_{response} \cdot \omega_j} \quad (54)$$

For the fundamental case $V_{j\max}$ will be considered as the maximum allowable error between the reference and the feedback, while for all the other frequencies $V_{j\max}$ is equal to the maximum allowable voltage harmonic, that is the voltage distortion at the respective harmonic frequency. The $I_{j\max}$ term represents the maximum output current harmonic that can be present in the load. The response time will have an important effect on the stability and performance of the overall system. A fast response time will quickly reduce the distortion but will require a higher gain; this could affect the overall stability. A long response time will require a lower gain but this might lead to large errors in the harmonic estimation; thus, the distortions will not be eliminated. It is clearly desirable to allow a much faster response for the fundamental component in order to avoid interactions with harmonic components. In order to correctly decouple the disturbance, one needs to compensate for the delay of the computation time and the delay of the power stage, which is usually approximated by a half switching period. Considering that the switching frequency is equal to half the sampling frequency as it is the case for the double-edged unsymmetrical PWM, the total delay that needs to be compensated for equals two sampling periods. Given the expression assumed for the disturbance $w_{1j}(k)$, it is easy to write the two samples ahead prediction as:

$$w_{1j}(k+2) = \cos(2\omega_j T)w_{1j}(k) - \sin(2\omega_j T)w_{2j}(k) \quad (55)$$

Finally (55) gives the estimation of the predicted output current harmonic component by solving a second order normal IIR filter. This can be seen as a linear combination of the current and voltage of a fictive resonant LC that satisfies (46) and tuned to the harmonic frequency. Of course, in practice there will be numerous errors that can affect the overall performance of the system. An integrating controller for the output voltage shown Fig. 3 is aimed toward nullifying the effects of finite-word effects, imperfect load disturbance,

parameter variation, inverter dynamics, etc. For a given standard DC integrating controller as given in (56), the expression for the equivalent AC integrating controller is given by (57) [1]:

$$H_{DC}(s) = \frac{K_{DC}}{s} \quad (56)$$

$$H_{AC}(s) = \frac{2K_{DC}s}{s^2 + \omega_1^2} \quad (57)$$

A good choice for the integrating constant of the AC controller is to select a value that would give the same or a certain percentage of the bandwidth for a standard DC controller. For equal bandwidths, replacing s with $j\omega_b$ in (56), (57) and K_{DC} with K_{AC} in (57) one obtains the following simple relation, where ω_b , ω_1 are the bandwidth and the fundamental frequencies respectively:

$$K_{AC} = \frac{\omega_b^2 - \omega_1^2}{2\omega_1^2} K_{DC} \quad (58)$$

It is important to mention however that the implementation for this controller is identical to that of the output current observer for the fundamental frequency; therefore, only one-second order IIR filter with normal architecture tuned at 400 Hz is needed and the integrating constant is made up the sum of c_1 and K_{AC} . A final computer simulation for the overall system including the output current harmonic observers can now be performed to ensure the overall stability and it might require fine adjusting of the integrating constants c_j .

V. THREE-PHASE APPLICATIONS

The proposed digital method has been analyzed for a single-phase inverter however three-phase applications are also possible. For low to medium power a typical three-phase inverter is shown in Fig. 6, while for very high power three single-phase inverters as in Fig. 1 are used in order to lower the stress on each semiconductor. Typically delta-star transformer isolation is used. For some high power applications it may be useful to employ a delta-zigzag structure that can better tolerate possible homopolar current components especially during the transients. The case where three single-phase inverters are used is straightforward; therefore, we will only consider the standard three-phase inverter depicted in Fig. 6. The analysis of this case can simply be reduced to that of two single-phase inverters as shown in Fig. 1 following a simple transformation from abc-coordinates to $\alpha\beta$ -coordinates as in (59a) and (59b):

$$y_\alpha = y_a \quad (59a)$$

$$y_\beta = \frac{y_b - y_c}{\sqrt{3}} \quad (59b)$$

In the above equations $y_{a,b,c}$ stand for the three-phase line voltages and inductor currents while y_α and y_β are the quadrature components of the same signals. It is not necessary to make the transformation to the rotating frame [7] since as pointed out before the use of the resonant controller for the output voltage ensures zero phase and amplitude errors. The use of AC signals enables us to directly eliminate the

distortion due to unsymmetrical loads without using separate regulators for the positive and negative sequences [8].

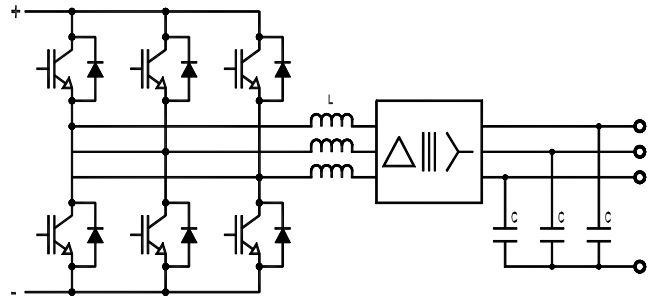


Fig. 6. Three-phase inverter with transformer isolation.

VI. EXPERIMENTAL RESULTS

The proposed digital method has been implemented using a 16-bit DSP-based controller ADMC401 (Analog Devices). This 26 MIPS single-chip DSP controller is well suited for the easy and inexpensive implementation of various high performance digital control algorithms because it includes all the facilities required in a voltage and current control loop such as: 12-bit flash A/D with 1.8 μ sec conversion time for all 8 channels, 6 channels with a 16-bits resolution PWM unit, two additional 8-bits PWM channels, 1-kbyte RAM for data memory, 2-kbyte RAM for program memory, 2-kbyte ROM program memory for boot routines and debug features, 2 event capture channels, encoder interface, 12 I/O channels etc. A single-phase 400 Hz, 115V IGBT based inverter rated for 10-KVA with a nominal DC-link voltage of 300V switching at 16 kHz was used to verify the proposed control method. The parameters of the filter are: $L = 100\mu$ H, $C = 50\mu$ F and in the first setup, the nonlinear load consisted of a full-wave diode bridge rectifier with an electrolytic capacitor of 3300 μ F and load resistance of 12 ohm. In all cases the THD was measured using a FLUKE 43B Harmonic Analyzer. The sampling frequency was chosen at 32 kHz and the PWM pulses are updated twice per carrier (double edged unsymmetrical PWM) in order to minimize the computational delay. Figure 7 depicts the output voltage and output current with a nonlinear load ($P = 2$ KW, $S = 3.2$ KVA, $R = 2.5$ KVAR) when all the output current observers are enabled. It can be seen from Fig. 6 that the THD is kept to a remarkable low value of 1.9%. The current in this case is 27 amps rms and the crest factor is 3.5.

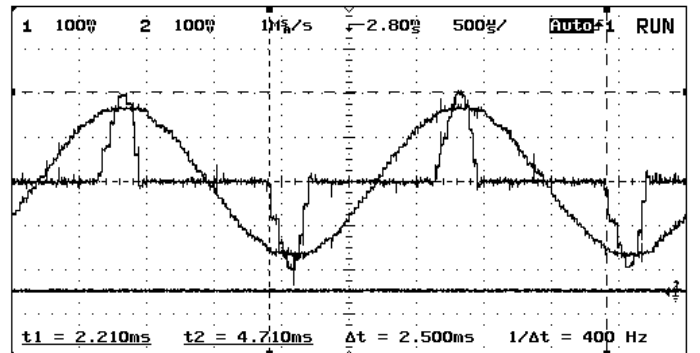


Fig. 7. Voltage (100V/div) and current (50A/div) with all output current observers enabled.

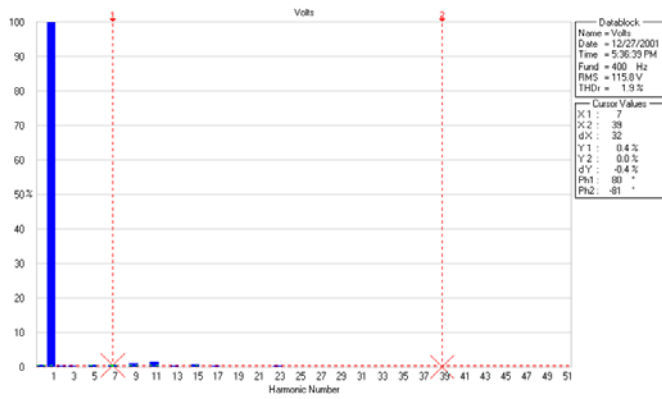


Fig. 8. Harmonic spectrum with all output current observers enabled.

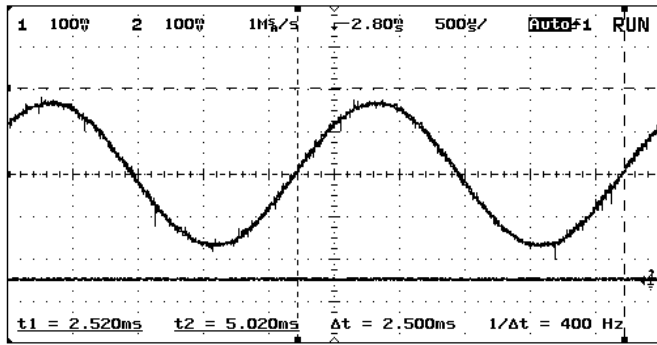


Fig. 9. Voltage reference and voltage feedback with nonlinear load (100V/div)

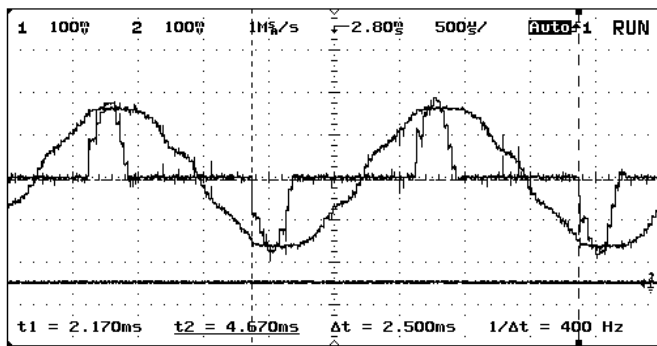


Fig. 10. Voltage (100V/div) and current (50A/div) with 7th harmonic current observer disabled.

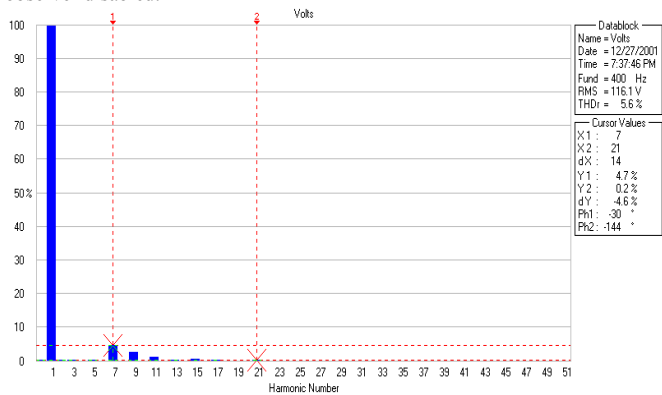


Fig. 11. Harmonic spectrum with the 7th harmonic current observer disabled.

The third, fifth and seventh harmonics are also almost completely eliminated, being kept to less than 0.4% by their

respective observers. Fig. 9 displays the feedback and reference voltages during the same nonlinear regime, and we can see an almost perfect overlapping, which shows that the phase and amplitude errors are almost zero. In Fig. 10, the observer for the 7th harmonic is disabled and the harmonic spectrum from Fig. 11 indicates that the THD has risen to 5.6% due to the increase in the 7th harmonic percentage (4.7%). If we disable also the observers for the fifth harmonic, the harmonics are increased even further as seen in Fig.'s 12 and 13 where the THD is now 8.3 % mainly due to the increase in the 5th harmonic component (8%). Finally, Fig.'s 14 and 15 depict the situation when all the output current observers for the harmonics (3rd, 5th, and 7th) are disabled and, as expected, the THD becomes increased to 16.3% with a large third harmonic of almost 16%.

A second setup was next considered where the nonlinear load consisted of a full bridge diode rectifier, an electrolytic capacitor of 200 μ F and load resistance of 3 ohm ($P = 5$ KW, $S = 6.4$ KVA, $R = 4$ KVAR). The voltage and current waveforms are depicted in Fig. 16; it can be observed that the voltage waveform is still very good although the current has risen now to 55.7 amps rms with a crest factor of 2.1. Fig. 17 depicts the voltage reference and the voltage feedback where only very minor distortion is seen but the phase error is still almost zero. The harmonic spectrum shown in Fig. 18 indicates a slight increase up to 2.4% but this is due to the ninth harmonic. This is not surprising since there is no observer for the ninth harmonic output current and the distortion generated cannot be compensated. Note, however, that the third, fifth, and seventh harmonics are still maintained at an extremely low level, less than 0.4 volts due to the correct estimation of the respective observers.

VII. CONCLUSIONS

This paper has presented a fully digital method suitable for single-phase and three-phase 400Hz inverters used in aircraft applications. The method proposes a fully decoupled method that includes a digital model of the inverter and involves the estimation of the main output current harmonics (third, fifth and seventh) through second order normal IIR filters. The control method is implemented on a 16-bit fixed-point single chip DSP-based controller from Analog Devices (ADMC401) and tested on a single-phase 10kva IGBT-based inverter prototype showing almost complete elimination of the third, fifth and seventh harmonics from the output voltage.

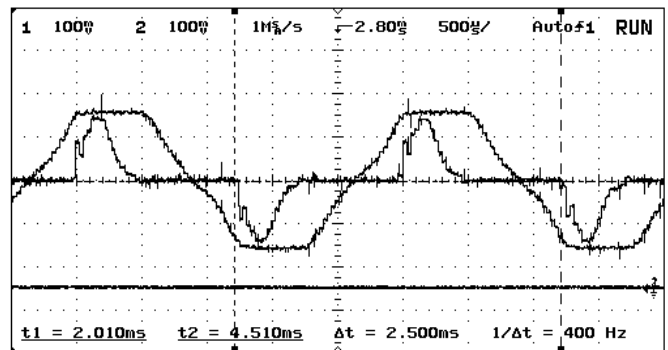


Fig. 12. Voltage (100V/div) and current (50A/div) with 5th and 7th harmonic current observers disabled.

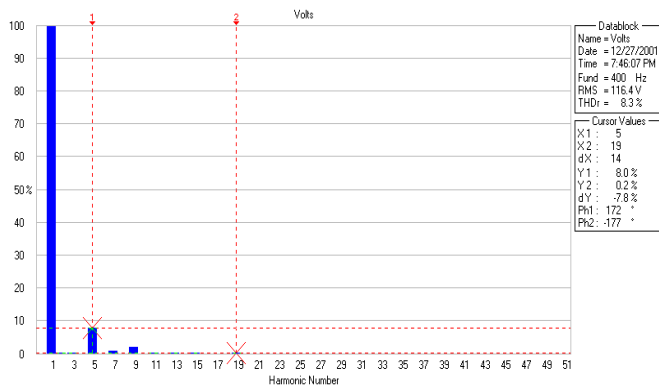


Fig. 13. Harmonic spectrum with the 5th and 7th harmonic current observers disabled.

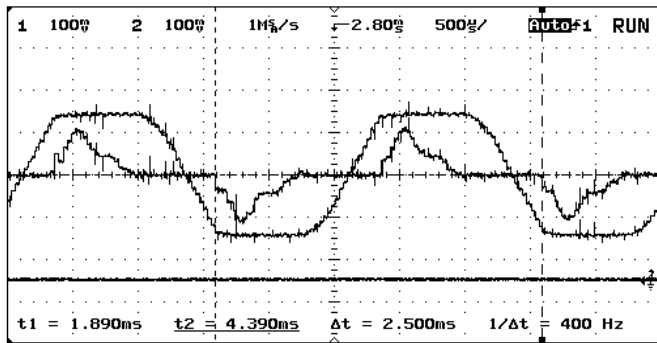


Fig. 14. Voltage and current (50A/div) with 3rd, 5th and 7th harmonic current observers disabled.

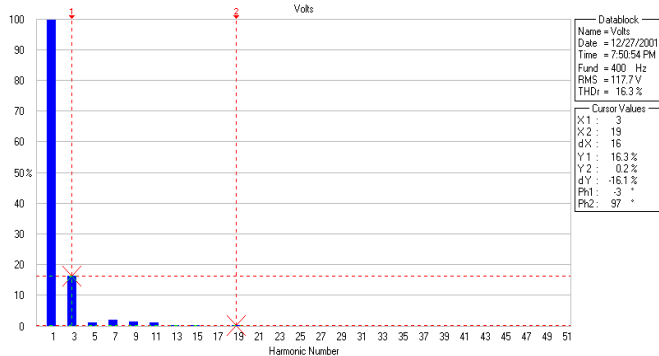


Fig. 15. Harmonic spectrum with the 3rd, 5th and 7th harmonic current observers disabled.

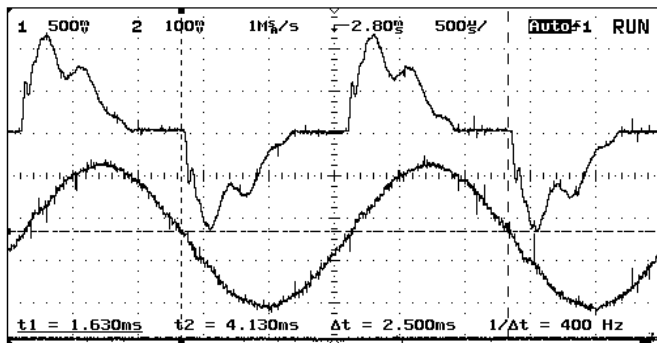


Fig. 16. Current (top 50 A/div) and voltage (bottom 100V/div) for the second setup (P = 5 KW, S = 6.4 KVA, R = 4 KVAR), with all current observers enabled.

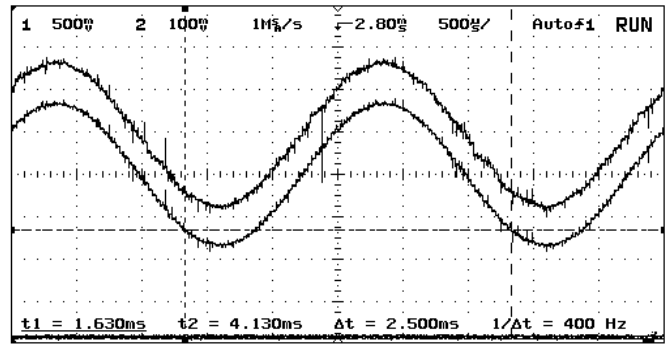


Fig. 17. Voltage feedback (top) and voltage reference (bottom), (P = 5 KW, S = 6.4 KVA, R = 4 KVAR) with all current observers enabled.

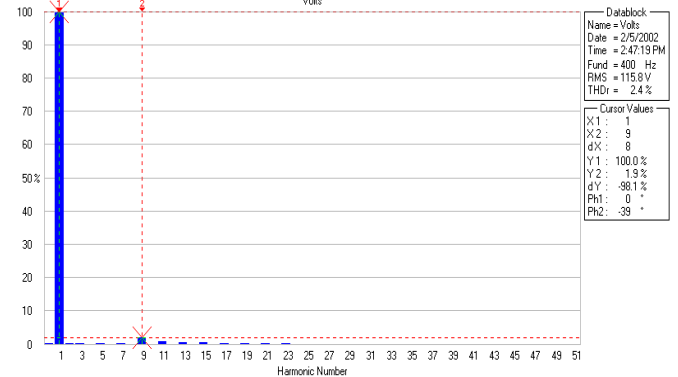


Fig. 18. Harmonic spectrum, (P = 5 KW, S = 6.4 KVA, R = 4 KVAR) with all current observers enabled.

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